Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An electrical structure, comprising:
a semiconductor device, the semiconductor device comprising a primary inverting amplifier and a programmable damping resistor; and
a crystal electrically coupled to the primary inverting amplifier, a resistance value of the programmable damping resistor being adapted to vary in order to control an amount of current flow from the primary inverting amplifier to the crystal, the amount of the current flow to the crystal being dependent upon electrical properties of the crystal.

[c2] 2. The electrical structure of claim 1, further comprising a first capacitor, a second capacitor, and a second resistor, wherein a voltage gain of the primary inverting amplifier is variable, and wherein the voltage gain of the inverting amplifier is adapted to be varied dependent upon the electrical properties of the crystal, a capacitance value of the first capacitor, a capacitance value of the second capacitor, and a resistance value of the second resistor.

[c3] 3. The electrical structure of claim 2, wherein at least

one of the electrical properties of the crystal comprises a design frequency value of the crystal.

[c4] 4. The electrical structure of claim 3, wherein the design frequency value of the crystal is selected from a range of about 32 KHz to about 100 MHz.

[c5] 5. The electrical structure of claim 2, wherein at least one of the electrical properties of the crystal comprises a quality factor (Q factor) of the crystal.

[c6] 6. The electrical structure of claim 2, wherein at least one of the electrical properties of the crystal comprises a power dissipation value of the crystal.

[c7] 7. The electrical structure of claim 2, wherein the voltage gain of the primary inverting amplifier is adapted to be varied to achieve a target gain value selected from a range of about 10 decibels (dB) to about 30 dB.

[c8] 8. The electrical structure of claim 2, wherein the primary inverting amplifier internally comprises a plurality of secondary inverting amplifiers electrically connected in parallel, and wherein the voltage gain of the primary inverting amplifier is adapted to be varied by enabling at least one of the plurality of secondary inverting amplifiers.

[c9] 9. The electrical structure of claim 2, wherein the primary inverting amplifier internally comprises a plurality of secondary inverting amplifiers electrically connected in parallel, and wherein the voltage gain of the primary inverting amplifier is adapted to be varied by disabling at least one of the plurality of secondary inverting amplifiers.

[c10] 10. The electrical structure of claim 2, wherein the primary inverting amplifier internally comprises a plurality of secondary inverting amplifiers, wherein the plurality of secondary inverting amplifiers is divided into a plurality of groups, wherein each group comprises at least two of the plurality of secondary inverting amplifiers electrically connected in parallel, and wherein the voltage gain of the primary inverting amplifier is adapted to be varied by enabling or disabling at least one of said groups.

[c11] 11. A method, comprising:
providing an electrical structure comprising a semiconductor and a crystal, the semiconductor device comprising a primary inverting amplifier and a programmable damping resistor, the crystal being device electrically coupled to the primary inverting amplifier;
varying a resistance value of the programmable damping resistor in order to control an amount of current flow from the primary inverting amplifier to the crystal, the

amount of the current flow to the crystal being dependent upon electrical properties of the crystal.

[c12] 12.The method of claim 11, further comprising:
providing a first capacitor, a second capacitor, and a second resistor; and
varying a voltage gain of the primary inverting amplifier according to the electrical properties of the crystal, a capacitance value of the first capacitor, a capacitance value of the second capacitor, and a resistance value of the second resistor.

[c13] 13. The method of claim 12, wherein at least one of the electrical properties of the crystal comprises a design frequency value of the crystal.

[c14] 14. The method of claim 13, wherein the design frequency value of the crystal is selected from a range of about 32 KHz to about 100 MHz.

[c15] 15. The method of claim 12, wherein at least one of the electrical properties of the crystal comprises a quality factor (Q factor) of the crystal.

[c16] 16. The method of claim 12, wherein at least one of the electrical properties of the crystal comprises a power dissipation value of the crystal.

[c17] 17. The method of claim 12, further comprising varying the voltage gain of the primary inverting amplifier to achieve a target gain value selected from a range of about 10 decibels (dB) to about 30 dB.

[c18] 18.The method of claim 12, further comprising:
providing within the primary inverting amplifier, a plurality of secondary inverting amplifiers electrically connected in parallel; and
varying the voltage gain of the primary inverting amplifier by enabling at least one of the plurality of secondary inverting amplifiers.

[c19] 19.The method of claim 12, further comprising:
providing within the primary inverting amplifier, a plurality of secondary inverting amplifiers electrically connected in parallel; and
varying the voltage gain of the primary inverting amplifier by disabling at least one of the plurality of secondary inverting amplifiers.

[c20] 20.The method of claim 12, further comprising:
providing within the primary inverting amplifier, a plurality of secondary inverting amplifiers, wherein the plurality of secondary inverting amplifiers is divided into a plurality of groups, wherein each group comprises at least two of the plurality of secondary inverting ampli-

fiers electrically connected in parallel; and

varying the voltage gain of the primary inverting amplifier by enabling or disabling at least one of said groups.